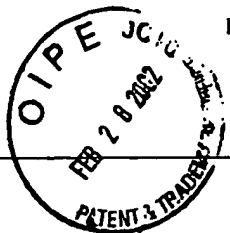


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56, §1.97, and §1.98 <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;">  </div> <div> PTO-1449 FORM SHEET 1 OF 1 </div> </div>				ATTORNEY DOCKET NO.: <div style="text-align: center;">025916-0238</div>		SERIAL NO.: <div style="text-align: center;">10/043933</div>	
				APPLICANTS: <div style="text-align: center;">Nedovic et al.</div>			
				FILING DATE: <div style="text-align: center;">January 11, 2002</div>			
				GROUP ART UNIT: <div style="text-align: center;">Not Assigned</div>			
U.S. PATENT DOCUMENTS							
† EX'R INITIAL	*REF. #	PATENT NUMBER	DATE (MO/YR)	NAME	U.S. CLASS/ SUBCLASS	FILING DATE (If appropriate)	
J	A1	US5764089	06/09/1998	H. Partovi et al.	327	08/30/1996	
J	A2	US5774005	6/30/1998	H. Partovi et al.	327	08/30/1996	
J	A3	US5898330	04/27/1999	E. F. Klass	327	06/3/1997	
J	A4	US5990717	11/23/1999	H. Partovi et al.	327	03/09/1998	
J	A5	US6087872	7/11/2000	H. Partovi et al.	327	2/23/1998	
J	A6	US5917355	06/29/1999	E. F. Klass	327	1/16/1997	
FOREIGN PATENT DOCUMENTS							
† EX'R INITIAL	*REF. #	PATENT NUMBER	DATE (MO/YR)	COUNTRY		TRANSLATION (YES/NO)	
OTHER DOCUMENTS							
† EX'R INITIAL	*REF. #	CITATION (Author, Article Title, Journal/Book Title, Date, Pertinent Pages, etc.)					
J	C1	H. Partovi et al., "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements", 1996 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, ISSCC, San Francisco, CA, USA, February 8-10, 1996.					
J	C2	B.-S. Kong, S.-S. Kim, Y.-H. Jun, "Conditional-Capture Flip-Flop Technique for Statistical Power Reduction" 2000 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 290-291, February 2000.					
J	C3	F. Klass, "Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic", Symp. on VLSI Circ. Digest of Technical Papers, June 1998.					
J	C4	J. Yuan, C. Svensson, "High-Speed CMOS Circuit Technique", IEEE Journal of Solid-State Circuits, Vol. 24, (No.1), pp. 62-70, February 1, 1989.					
J	C5	N. Nedovic, V. G. Oklobdzija, "Hybrid Latch Flip-Flop with Improved Power Efficiency", Proceedings of Symposium on Integrated Circuits and Systems Design, pp. 211-215, 2000.					
EXAMINER'S SIGNATURE <div style="text-align: center; font-size: 1.5em;">Vule</div>				DATE CONSIDERED <div style="text-align: center; font-size: 1.5em;">10/28/05</div>			
† EXAMINER: Initial if reference is considered, whether or not citation is in conformance with MPEP 609. Line through citation if not in conformance and not considered. Include copy of this form in next communication to applicant. * If an asterisk is placed beside the reference number, a copy is not provided because the reference was previously cited by or submitted to the PTO in a prior application that is identified in the statement and relied upon for an earlier filing date under 35 U.S.C. 120. 37 C.F.R. 1.98(d).							